REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claim 1

Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by Chou (U.S. Patent No. 6,674,317). Applicant has canceled claim 1 without prejudice or disclaimer. Applicant thus submits that the rejection under 35 U.S.C. § 102(e) is mooted.

Claims 29 and 33

Claim 29 and 33 were rejected under 35 U.S.C. § 102(b) as being anticipated by Liu (U.S. Patent No. 6,064,602). Applicant respectfully traverses.

The Office Action has identified pass gates 120 of Chou as corresponding to Applicant's pass gates. Claim 29 recites, in part, "applying a boosted voltage to gates of each of the nFET pass gates of the selected block, wherein the boosted voltage exceeds the programming voltage by at least one threshold voltage of the nFET pass gate and wherein the boosted voltage is generated by a single source." However, Chou expressly teaches that the voltage applied to the control electrode of the pass gates 120 should be less than its programming voltage. *See,* Chou, column 4, lines 12-14 ("Furthermore, the VW voltage should be at a sufficiently low level to isolate the high voltages on the word lines (provided by the HV coupler circuit) from the row decoders.").

In addition, there is no teaching that a boosted voltage applied to the gates of the pass gates is generated by a single source. In particular, Applicant notes that each row is supplied with its own HV coupler circuit 130. It is the HV coupler circuit 130 that determines whether the programming voltage Vpp is applied to a word line and each HV coupler circuit 130 appears to have its own pass gate that is not shown or described by Chou. *Cf.,* Chou, column 3, lines 45-54 ("Specifically, if the word line connected to the HV coupler circuit is at or above a selected VT(HV) voltage, then the HV coupler circuit place VPP on the word line"). Applicant contends that Chou does not teach or suggest that any voltage applied to a pass gate controlling whether Vpp is applied to a word line is a voltage generated from a single source.

Applicant has distinguished itself from prior solutions using local pass circuits to control application of programming voltages. *See,* Specification, paragraph 0046 ("In the various embodiments of the invention, by providing a voltage boosted from Vpp, a single pass circuit can be used to activate pass gates for multiple rows of a selected block. This is advantageous over local pass circuits where each pass gate of each row of the block is provided with its own pass circuit. Using pass circuits of the type described herein, a single pass circuit can provide a gate voltage to a number of pass gates where that gate voltage has a potential level that exceeds Vpp by at least the Vt of the pass gate. This will permit a clean passing of the programming voltage to the memory cells without requiring individual pass circuits for each row.").

Claim 33 recites, in part, "activating a pass circuit for each target block, each pass circuit receiving a programming voltage," "generating a boosted voltage on an output of each activated pass circuit, wherein the boosted voltage has a voltage level that exceeds the programming voltage," "providing each boosted voltage to a plurality of pass gates, each pass gate coupled to a row of a target block" and "providing the programming voltage to each target row through its associated pass gate receiving the boosted voltage."

Similar to the issues noted with respect to claim 29, the pass gates 120 of Chou do not correspond to the pass gates as recited in claim 33. The pass gates 120 of Chou do not each receive a programming voltage. The programming voltage is only received at a pass gate 120 if it has placed a particular voltage on its corresponding word line. *See,* Chou, column 3, lines 45-54. A boosted voltage is not generated on an output of voltage booster 140 of Chou. *See,* Chou, column 4, lines 12-14. And the programming voltage is not provided to a row of memory cells 105 through its associated pass gate 120. As shown in Figure 1, the programming voltage is applied to the rows of memory cells 105 from a side opposite the pass gates 120 as opposed to being applied through the pass gates 120.

In view of the foregoing, Applicant respectfully submits that claims 29 and 33 are patentably distinct from the cited reference. Applicant thus requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b), and allowance of claims 29 and 33.

Allowable Subject Matter

Claims 2-5 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Applicant has amended claims 2-5 as suggested by the Examiner. Applicant thus respectfully requests reconsideration and withdrawal of the objection, and allowance of claim 2-5.

Allowed Subject Matter

Applicant acknowledges that claims 6-28, 30-32 and 34-45 were indicated to be allowed.

CONCLUSION

Claim 1 is canceled hereby without prejudice or disclaimer. Claim 2 is amended herein. Claims 2-45 are now pending.

Applicant believes that the claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions regarding this application, please contact the under-signed at (612) 312-2204. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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